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Dataflow Graph Partitioning for High Level Synthesis

Abstract

This paper presents a **dataflow graph (DFG) partitioning algorithm for effective high level synthesis** in the presence of constraints like data **initiation interval (II) and area**. It also focuses on handling large DFGs for high level synthesis with area reduction as a requirement. The algorithm works so as to fit a design into the design space between a fully pipelined design and a fully resource shared design in order to meet the initiation interval constraint and reduce area ***only as much as required.*** .

Claims

To the best of our knowledge the work presented here is the first to:

•Investigate partitioning of DFG for implementation on a single FPGA under II constraint and area considerations without reconfiguration

•Investigate effective management of large DFGs under II constraint and area considerations

Motivation

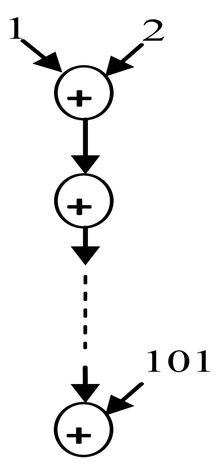

Fig 1. A large DFG

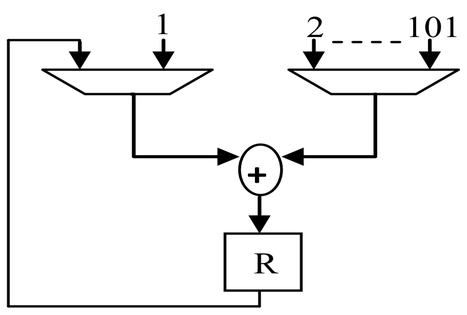

Fig 2. A typical resource shared datapath for DFG in Fig .1 based on traditional hardware binding algorithms

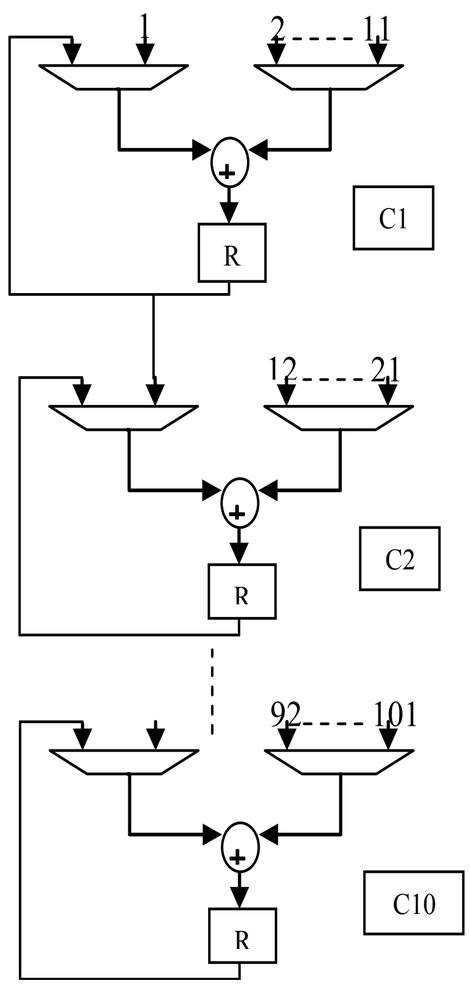

Fig 3. Datapath for II = 4 clock cycles for DFG in Fig. 1

Datapath Design	Area	Functional for II=4	Comments
As in Fig. 1	Max	Yes	Wastage of resources (adders) as primary input data (1 & 2) arrives only every 4 clock cycles and not every clock cycle for which the design exists in current form
As in Fig. 2	Min	No	A new set of primary input data (1&2) can be fed only after all 100 additions have been completed
As in Fig. 3	Min < Area < Max	Yes	Resource (adder) is shared to reduce area and II constraint is also met

II Aware DFG Partitioning

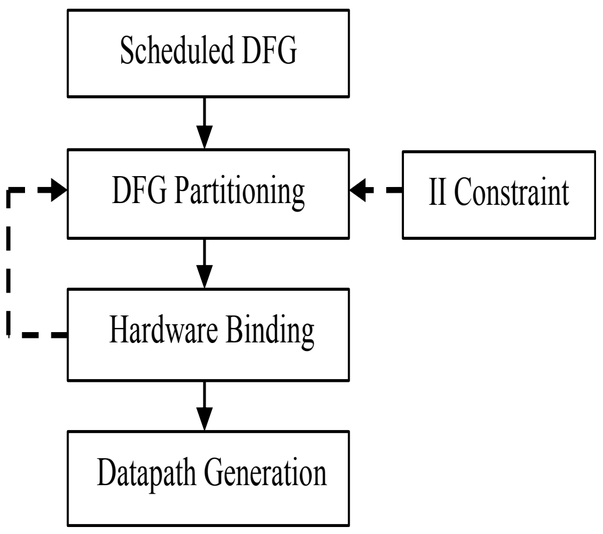

Fig 4. HLS flow with DFG partitioning

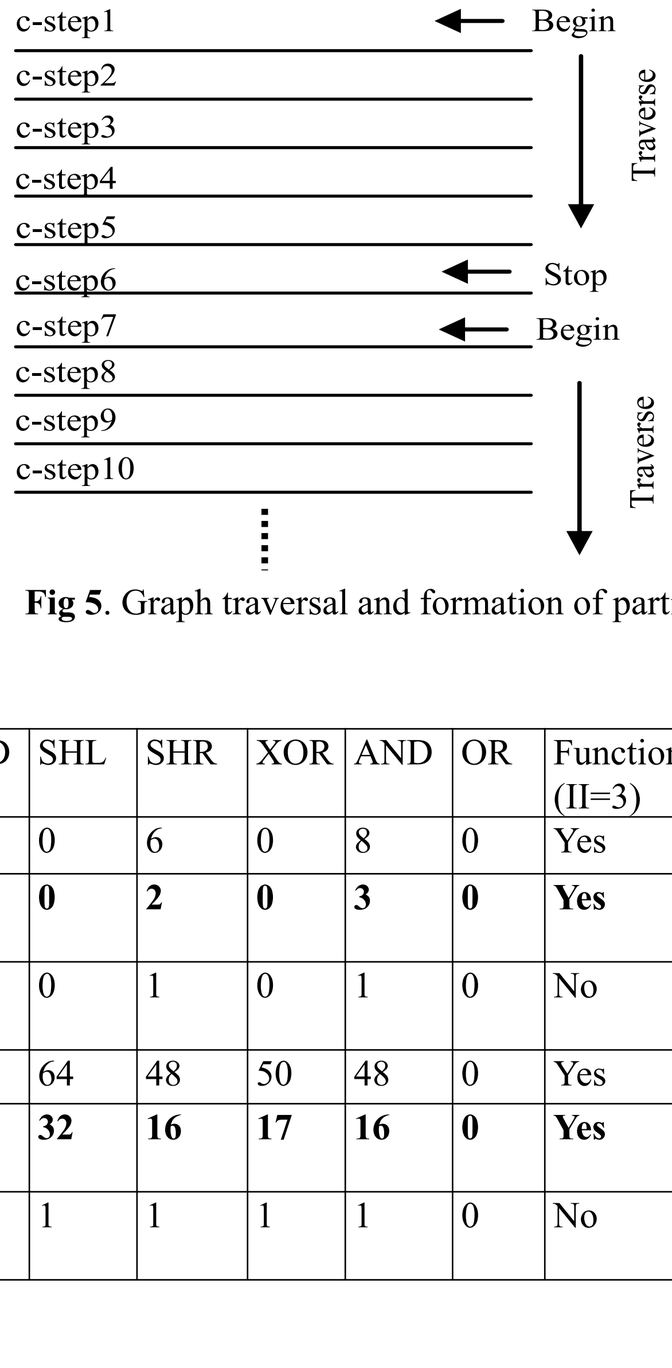

Fig 5. Graph traversal and formation of partitions

Results

MediaBench		# c-steps	ADD	SHL	SHR	XOR	AND	OR	Functional? (II=3)
Blowfish_cbc	Original	14	0	0	6	0	8	0	Yes
	II-aware partitioned	**14**	**0**	**0**	**2**	**0**	**3**	**0**	**Yes**
	Without partitioning	14	0	0	1	0	1	0	No
Blowfish_bf_enc	Original	354	144	64	48	50	48	0	Yes
	II-aware partitioned	**354**	**48**	**32**	**16**	**17**	**16**	**0**	**Yes**
	Without partitioning	354	1	1	1	1	1	0	No

References

[1] U. Dhawan, S. Sinha, et al. "Extended compatibility path based hardware binding algorithm for area-time efficient designs", in Proc.2nd Asia Symp. Of Quality Electronics Design, August 2010, Penang, pp. 151-156.

[2] Y. C Jiang and J.F. Wang, "Temporal partitioning dataflow graphs for dynamically reconfigurable computing", IEEE Trans. on VLSI, vol. 15, no. 12, pp. 1351-1361, Dec. 2007

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