Using DSP Block Pre-adders in Pipeline SDF FFT Implementation in Contemporary FPGAs

Carl Ingemarsson, Petter Källström and Oscar Gustafsson

Linköping University
INSTITUTE OF TECHNOLOGY
Linköping University
Department of Electrical Engineering

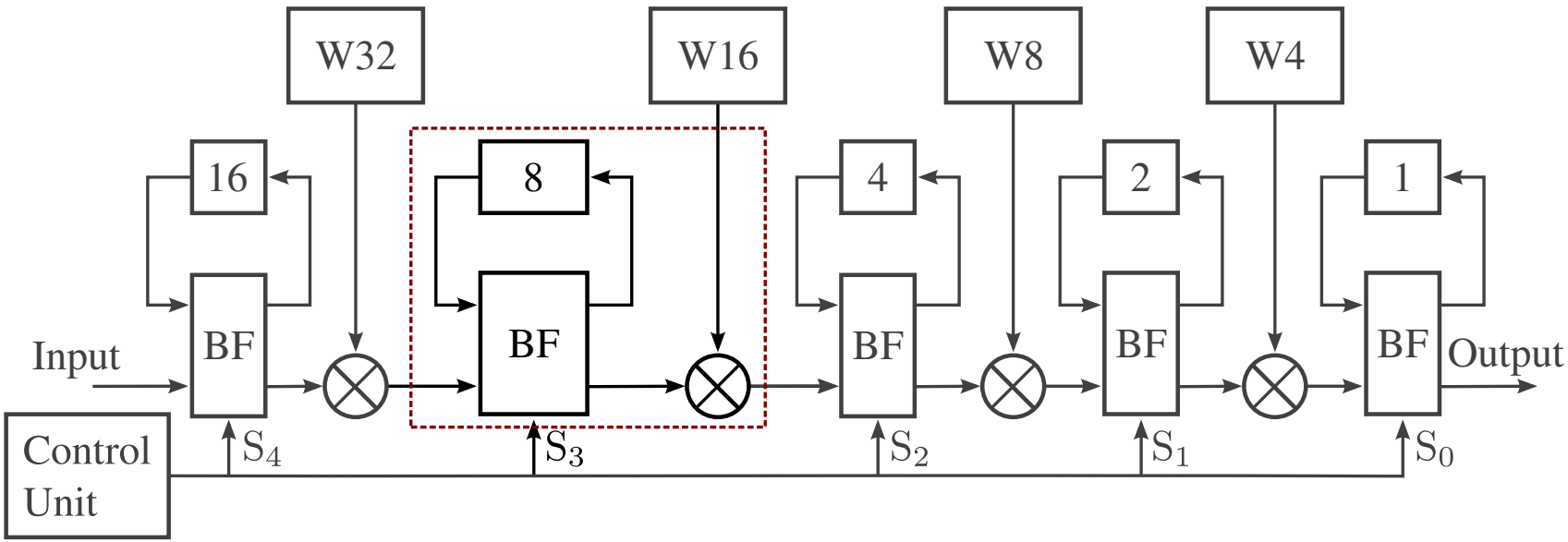
Outline

Using DSP Block Pre-adders in Pipeline SDF FFT Implementation in Contemporary FPGAs

Introduction

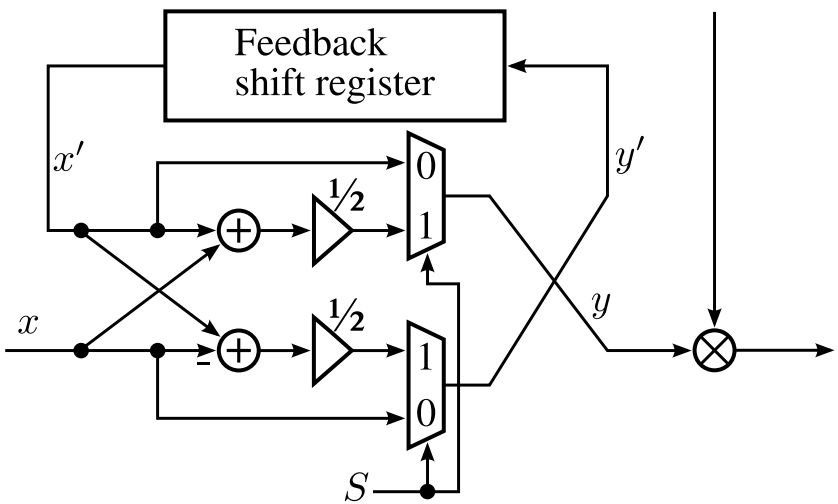
- DFTs are widely used in, e.g., OFDM communications.
- Straight forward implementation of FFT is common.
- This implementation is not efficient in FPGAs.
- We have mainly focused on the 6 and 7 series Xilinx FPGAs.

Radix-2 SDF FFT Structure

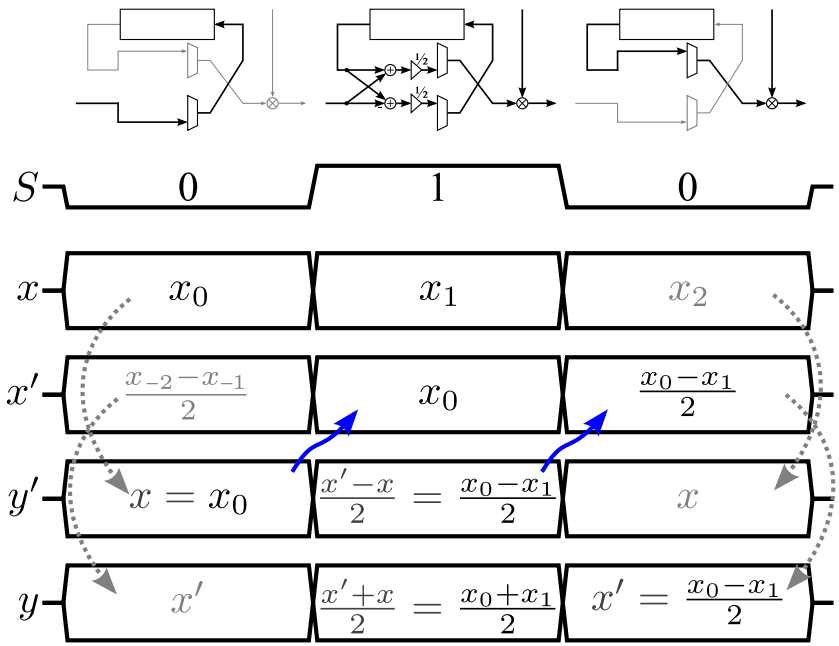


Entire structure of a 64 point radix-2 SDF FFT processor.

One stage



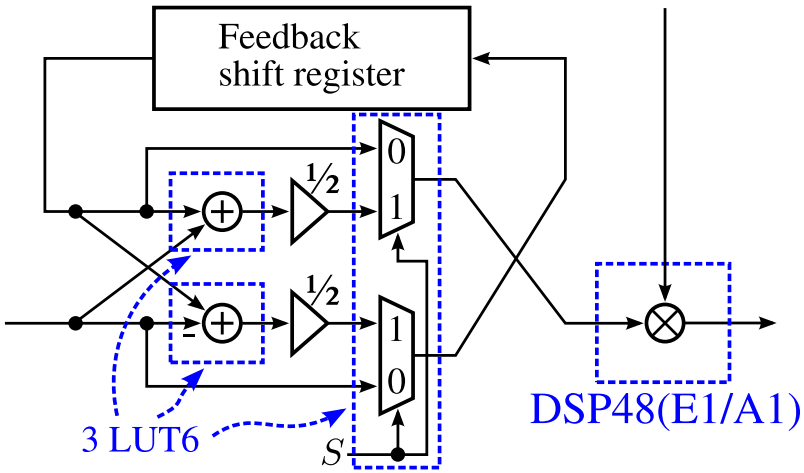
One stage



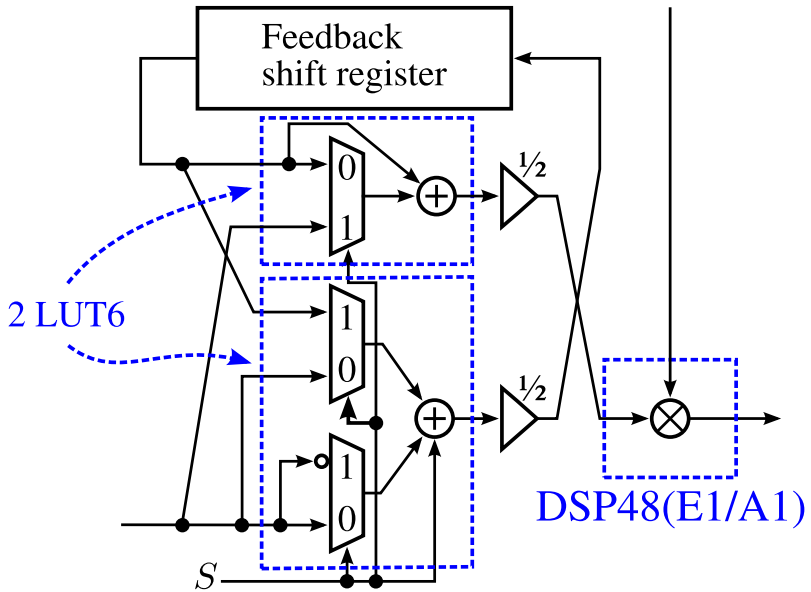
Data flow

Original structure of one stage of the FFT architecture.

First Optimization



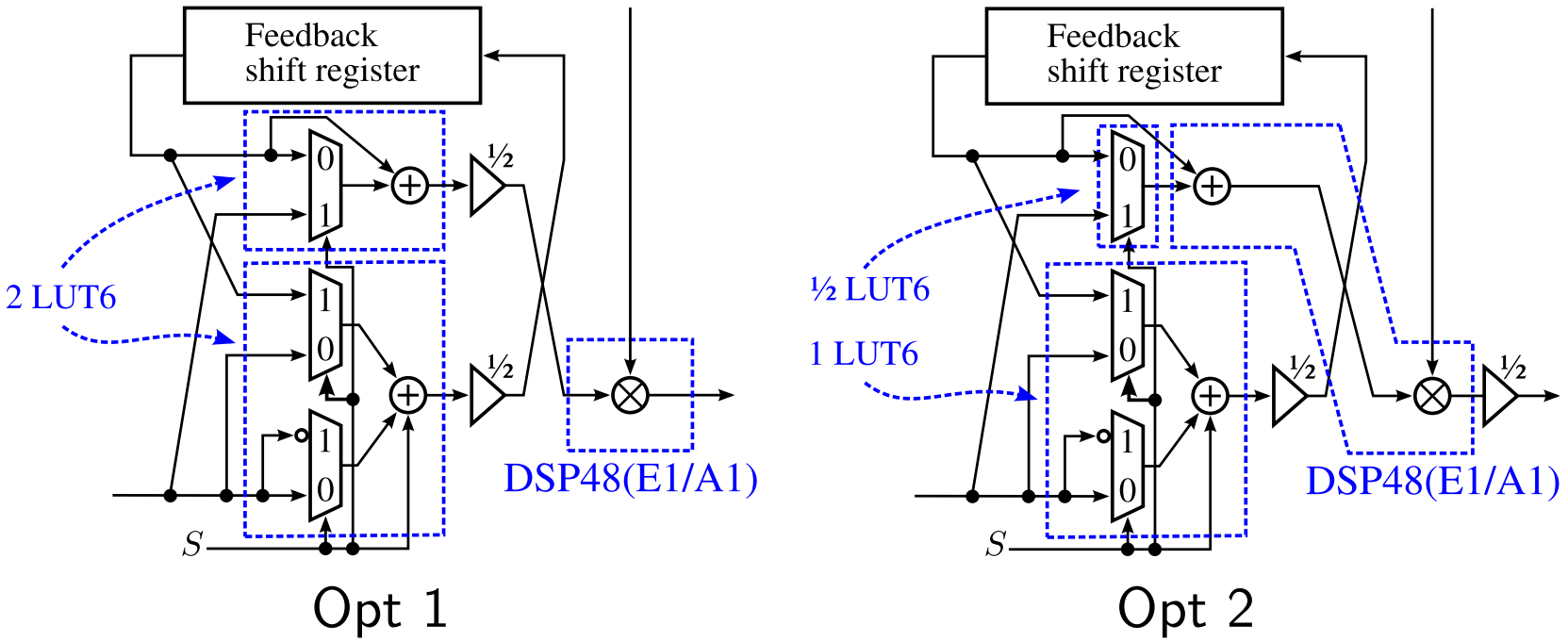
Original



Opt 1

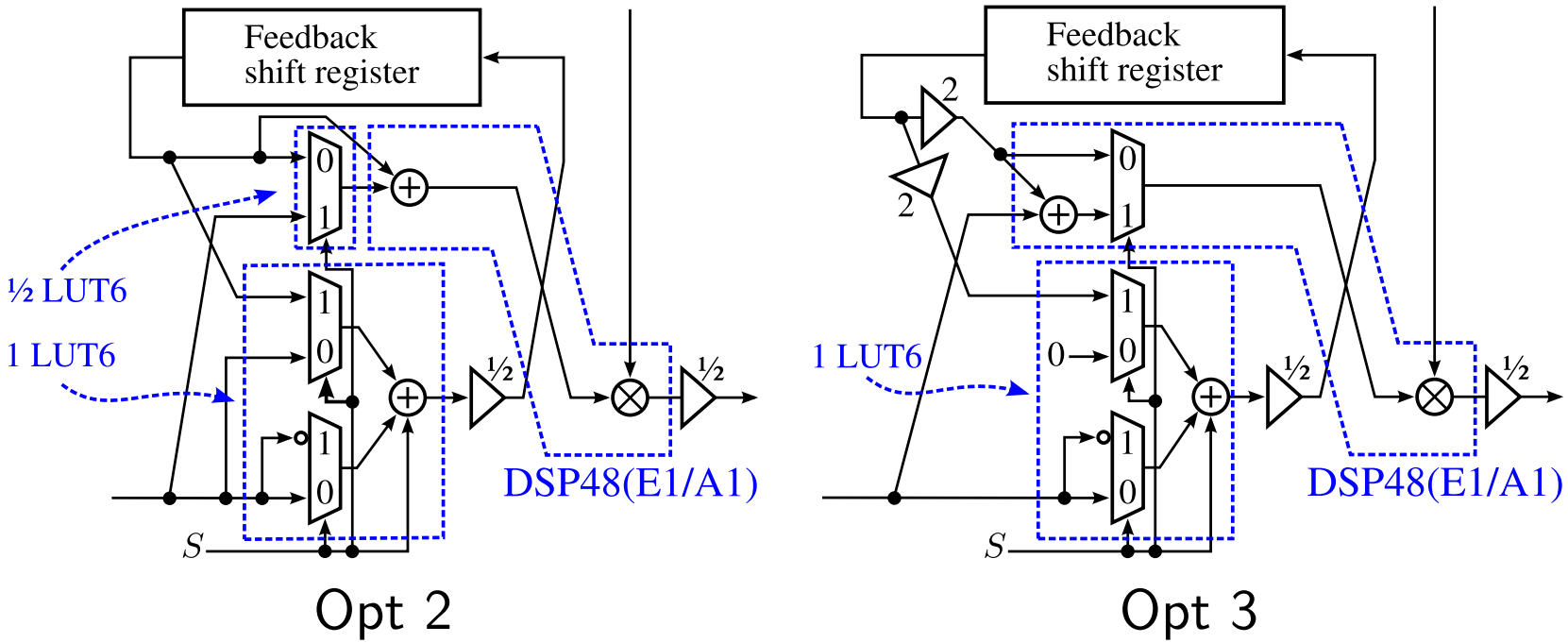
Key transformation relation: $X = \frac{X+X}{2}$.

Second Optimization



Utilizing the existing pre-adder in the DSP-blocks.

Third Optimization



If the pre-adder has a bypass function, this allows a third transformation, affecting the content in the shift register.

Optimization Summary

Resource usage with respect to word length W.

	# LUTs	# DSP48s
Original	$W \times 6$	4
Optimization 1	$W \times 4$	4
Optimization 2	$W \times 3$	4
Optimization 3	$W \times 2$	4

One extra bit in each adder, used for sign extension, is required, using one LUT each (4, 4, 2, 2 in the designs, respectively).

Implementation Results

Implementation results for 16 bit word length in a Xilinx Virtex 6 (xc6vsx315t).

	# slices	# LUTs	# DSP48E1s	Expected
Original	44	116	4	$16 \cdot 6 + 4 = 100$
Opt. 1	20	68	4	$16 \cdot 4 + 4 = 68$
Opt. 2	21	50	4	$16 \cdot 3 + 2 = 50$
Opt. 3[1]	10	34	4	$16 \cdot 2 + 2 = 34$

[1] Manual placement required.

Expected number of LUTs includes sign extension in additions.

Applicability to Other FPGAs

- Optimization 1 can be applied to most FPGAs.
- Optimization 2 utilizes the pre-adder of contemporary FPGAs.
- Optimization 3 needs a pre-adder with bypass functionality.

Conclusion

- We have proposed transformations of a radix-2 SDF stage.
- These transformations reduce the LUT usage and utilize pre-adders of the DSP blocks.
- This is applicable to Xilinx' 6 and 7 series FPGAs, but should be usable also in other FPGA families.

Thank you

Thank you.
Any questions?