DUAL-CORE MOTION ESTIMATION PROCESSOR

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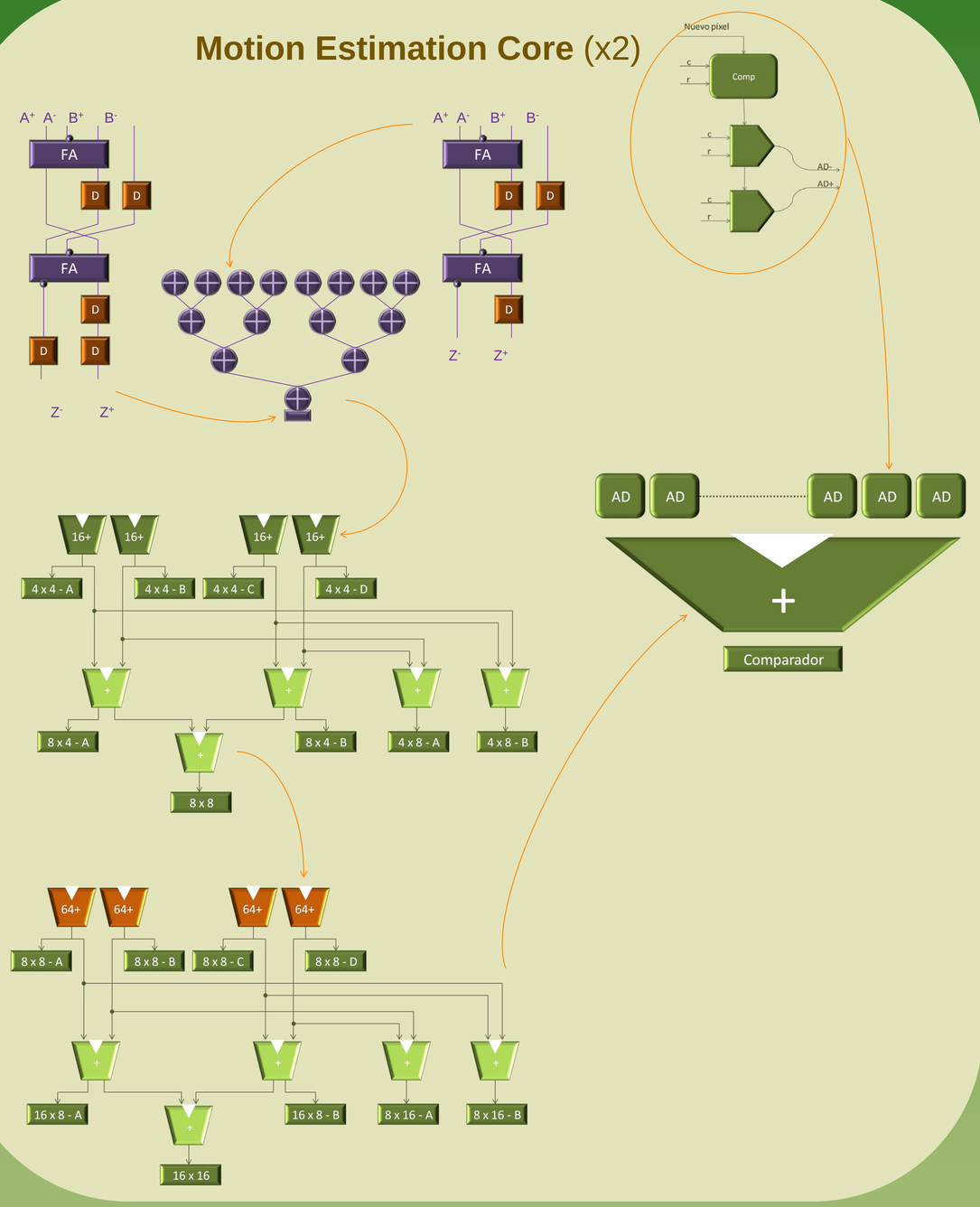
ABSTRACT

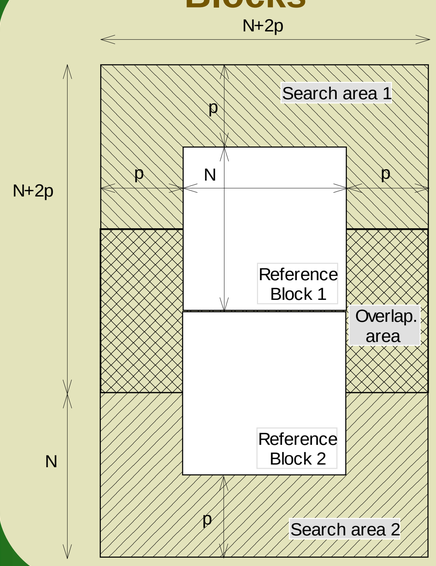
This paper presents a motion estimation processor based on a dual-core architecture. Both cores are based on bitserial adder trees. Memory structures are also described.

This architecture is bit-precision reconfigurable. Performance results for several smartphones and tablets are presented. Furthermore, hardware results and comparison with other works are included. Real-time processing is achieved for all devices studied.

Motion Estimation Core (x2)



Blocks



Arithmetic:

Signed Digit Radix 2

Value	SD
+1	01
0	00
0	11
-1	10

Comparison with other works

Architectures	Area (gates)	Throughput Performance (MB/s)	(MB/s)/gate
[4]	67.7k	64.9k	0.959
[5]	175k	31.7k	0.181
[6]	160k	159k	0.996
[7] NTB=0	**54k**	77.4k	1.433
[7] NTB=4	54k	101.2k	1.874
NTB=0	112k	184.2k	1.645
NTB=4	112k	**245.6k**	**2.193**

Scores

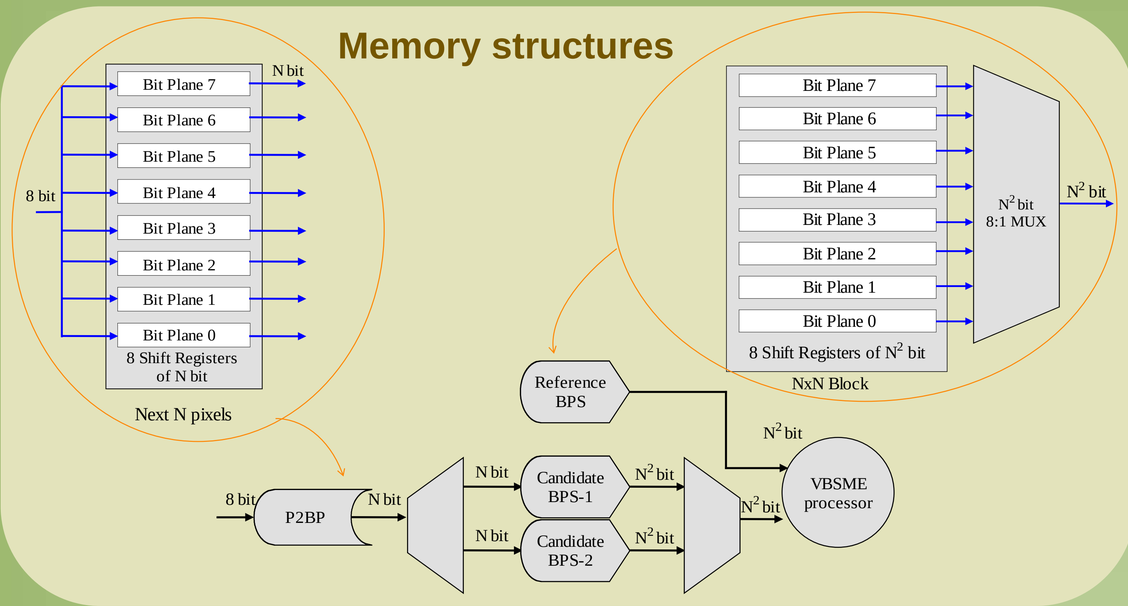
Kintex-7 FPGA

Processors: 6361 Slices

G.System: 16689 Slices

425.8 MHz

Memory structures



Throughput in Smartphones (fps)			# Truncated Bits (NTB)			
Smartphone	Resolution	Aspect Ratio	0	2	4	6
Several	QVGA 320×240	4:3	613.9	701.6	818.5	982.2
iPhone 3	HVGA 480×320	3:2	307.0	350.8	409.3	491.1
BlackBerry Torch 9800	HVGA+ 480×360	4:3	272.8	311.8	363.8	436.6
Nokia N8 – N97	nHD 640×360	16:9	204.6	233.9	272.8	327.4
HTC Touch Pro	VGA 640×480	4:3	153.5	175.4	204.6	245.6
Nokia Lumia; Galaxy R–S	WVGA 800×480	5:3	122.8	140.3	163.7	196.5
HTC Radar – HTC 7 Mozart						
Apple iPhone 4	960×640	3:2	76.7	87.7	102.3	122.8
Samsung Galaxy Tab	WSVGA 1024×600	–	76.7	87.7	102.3	122.8
Apple iPad XGA	1024×768	4:3	60.0	68.5	79.9	95.9
Samsung Galaxy Nexus	HD720 1280×720	16:9	51.2	58.5	68.2	81.9
Samsung Galaxy Tab 10.1	WXGA 1280×800	8:5	46.0	52.6	61.4	73.7

CONCLUSION

A new reconfigurable architecture to process the VBSME for H.264/MPEG-4 AVC standard is presented.

The SD representation does not require processing time for the conversion, or any extra memory cost: the conversion from two's complement representation to SD is carried out at the same time as the absolute difference processing, simplifying the computation.

There is not a conversion from SD to two's complement due to the fact that the SAD value is only used to calculate the MV. The on-chip memory is the same that will be needed for processing in two's complement representation. In future, compression proposed in [8] could be applied.

The presented ME architecture is designed for bit-serial computation, and does not depend on the pixel width, which facilitates an easy reconfiguration of the device in real-time, and allows to save computing time, in fact 25% of it can be saved for NTB=4. Furthermore, NTB can be reconfigured while the smartphone is operating to save processing, extending battery life.

The low cost, the reduced on-chip memory, and the high throughput makes this architecture suitable for resource-limited systems.

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