Beyond Moore.
Beyond Programmable Logic.

Steve Trimberger
Xilinx Research
FPL  30 August 2012
Beyond Moore.
Beyond Programmable Logic.
Agenda

- What is happening in semiconductor technology?
  - Moore’s Law
  - More than Moore
  - Less than Moore?

- What is happening at Xilinx?
  - How Xilinx is dealing with the latest in semiconductor technology
  - Technology and product trends
  - The latest round of devices and technologies
  - It is not just logic anymore

- What will happen next?
Part 1. Is Moore’s Law Ending?
Part 1. Is Moore’s Law Ending?

Railroad Track 1820-1890

Goetz, Transvision 8/2004
Nothing New: Power Challenge

Challenge 1: Power

Power Density Race

Multi-Core

Source: Intel
Nothing New: I/O Bandwidth Gap

Multi-Gigabit Transceivers

Source: Xilinx, Inc.
The main message in 2011 remains—Cost (of design) is the greatest threat to continuation of the semiconductor roadmap.” ITRS 2011
Moore’s Law: The Technology Pipeline

<table>
<thead>
<tr>
<th>$V_{dd}$</th>
<th>1.0/1.1V</th>
<th>0.9/1.0V</th>
<th>0.8/0.9V</th>
<th>0.7/0.8V</th>
<th>0.6/0.7V</th>
<th>0.5/0.6V</th>
<th>&lt; 0.5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced Gate Stack Engineering</td>
<td>Fully-depleted Channel Electrostatics</td>
<td>Band-Engineered Channel for Enhanced Transport</td>
<td>New Transport &amp; Extreme Channel Electrostatics</td>
<td>2D Quantum Materials</td>
<td></td>
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</tbody>
</table>

Tech Node

- 32/28nm
- 22/20nm
- 10nm
- 5nm

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Industry Debates Variability and Reliability

EE Times
IMEC looks at variability beyond 10 nm
Anne-Françoise PELE
6/1/2012 5:10 PM EDT
PARIS – CMOS technology scaling will go on for the foreseeable future but, as we enter the 10nm node, process complexity reduction and variability control will become crucial and drive technology decisions, said An Steegen, senior vice president process technology at imec, at the annual IMEC Technology Forum last week at the Square meeting center in Brussels, Belgium.

EE Times
Intel FinFETs vary, may need SOI for shrink, says GSS
Peter Clarke
6/6/2012 7:01 AM EDT
LONDON – Intel’s 22-nm FinFETs show physical variability according to cross-sectional photographs from engineering consultancy Chipworks Inc. (Ottawa, Ontario) and EDA company Gold Standard Simulations Ltd. (GSS) has attempted to model electrical characteristics of various examples.

One conclusion drawn by Professor Asen Asenov, CEO of GSS (Glasgow, Scotland), is that Intel may need to turn to silicon-on-insulator wafers to scale its yet to introduce FinFET technology into their chip manufacturing processes.
Industry Debates Cost

COST PER GATE REDUCTION TRENDS

ARM 20nm Processors Expected to Arrive Next Year
Douglas Perry
6/5/2012 6:00 PM EDT
The chip manufacturing race is heating up and Intel could be pressure down the road.

Nvidia deeply unhappy with TSMC, claims 20nm essentially worthless
Joel Hruska
March 23, 2012 at 12:13 pm
One of the unspoken rules of customer-foundry relations is that you virtually never see the former speak poorly of the latter. Only when things have seriously hit the fan do partners like AMD or Nvidia

EE Times
TSMC raises capex to record $8.5 billion, pulls in 20-nm
Peter Clarke
4/26/2012 12:23 PM EDT
LONDON – Taiwan Semiconductor Manufacturing Co. Ltd. has raised its planned capital expenditure for 2012 to between $8 billion and $8.5 billion. The move accompanied the announcement of first quarter financial results and strong second quarter outlook by the foundry.
Moore’s Law Today

- We still get more transistors!
- Must trade performance for power savings
  - Dennard scaling ended around 2000
- Slow growth of I/O pins
  - I/O bandwidth requirements drive high-speed serial
- Less area improvement with each new node
  - Lithography limitations restrict layout
  - Quantized transistor sizes with FinFETs
- Process complexity and limited suppliers drive up wafer pricing and delay production price reductions
- We still get more transistors!
Part 2. What Is Xilinx Doing?
Expanding Programmable Technology Leadership

- Committed to be First to Process Nodes
- Pioneering 3-D IC Technology
- Leading Edge Processing Systems
- Programmable Analog/Mixed Signal
- System to IC Tools, IP, and Ecosystem

From Programmable Logic to Programmable Systems Integration

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FPGA Capacity Trend Looking Up

![FPGA Capacity Trend Graph](image)

- **Number of LCs**: 1.00E+02, 1.00E+03, 1.00E+04, 1.00E+05, 1.00E+06, 1.00E+07
- **Largest Xilinx FPGA**
FPGA Performance Trend Looking Up
FPGA Energy Trend Looking down
High-k Metal Gate Transistor in 28nm HPL Process

HKMG:
- introduced by Intel at 45nm
- available at 28nm from top foundries

> 25x lower gate oxide leakage
> 30% lower switching power
> 30% higher drive current or
> 5x lower source-drain leakage

Ground Breaking Capacity Gains at 28nm
World’s First 2 Million Logic Cell FPGA

- Over 2x capacity increase over Spartan-6 and Virtex-6 FPGAs

<table>
<thead>
<tr>
<th>Family</th>
<th>Capacity Range</th>
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<tr>
<td>ARTIX</td>
<td>8K – 350K LCs</td>
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<tr>
<td>KINTEX</td>
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- 8K – 2M LCs; the widest capacity range offered in a single unified product family

- Larger densities enable higher performance
  - More calculations/clock cycle by utilizing parallelism inherent in FPGAs
SSI Technology Harnesses Proven Technology in a Unique Way

- Microbumps
- Silicon Interposer
- Through-Silicon Vias
- C4 Bumps
- BGA Balls

28nm FPGA Slice

Through-Silicon Vias (TSV) (65nm Generation)

- Bumps leverages ubiquitous image sensor microbump technology
- 4 conventional metal layers connect microbumps & TSVs
- No transistors means low risk and no TSV induced performance degradation
- Etch process (not laser drilled)

Passive Silicon Interposer (65nm Generation)

- Access to logic regions
- Access to high density power / ground / IOs
- Coarse pitch, low density aids manufacturability

Side-by-Side Die Layout

- Minimal heat flux issues
- Minimal design tool flow impact
2.5D: Crossing the Chasm

- Very high bandwidth, low capacitance interconnections
- Known Good Die packaged
- “Large die” yield opportunity
Virtex 2000T: Homogeneous 3D

- 4-layer metal Si interposer with TSV
- 4 FPGA sub-die in package
- >10,000 inter-die connections
- 2 Million Logic Cells
- 6.8 Billion Transistors
Virtex-7 HT: Heterogeneous 3D

- Yield optimized
- Noise isolation
- 28G transceiver process optimized for performance
- FPGA logic process optimized for power

- 2.8Tb/s ~3X Monolithic
- 16 x 28G Transceivers
- 72 x 13G Transceivers
- 650 GPIO
3D: The Next Frontier

- What is inside?
- How high can we go?
- What is on top?

- High performance chip on top for thermal and TSV process availability
- Bottom die supports power TSV’s for top die (Swiss cheese) in older technology (TSV friendly)
- Floor-planning critical:
  - Thermal concerns (stacked thermal flux)
  - TSV keep out zones in bottom die to avoid stress-induced performance impact
- What about user-defined stacks?
Beyond Moore with SSIT

- Break the exponential cost of large die
- Break through pin limitations for higher bandwidth and lower power
- No more compromises for high-performance vs. low power for very high-speed I/O
Nothing New: Productivity Gap

Source: SEMATECH

System Integration Required

Source: SEMATECH
Hardware and Software Programmability

Estimated FPGA/PLD Design Starts, 2003-2013

Source: Gartner (March 2009), Report: Market Trends - ASIC Design Starts, 2009

- With Microprocessor Core
- Without Microprocessor Core
Xilinx Technology Evolution

Programmable Logic Devices
Enables Programmable ‘Logic’

ALL Programmable Devices
Enables Programmable Systems ‘Integration’
The Zynq™-7000 Processor+FPGA SoC

- **Complete ARM®-based Processing System**
  - Dual ARM Cortex™-A9 MPCore™, up to 1GHz
  - Supports multiple operating systems
  - Fully autonomous to the programmable logic

- **Tightly Integrated Programmable Logic**
  - Used to extend processing system
  - High performance AXI based interface
  - Scalable density and performance: 30K-350K LCs

- **Flexible Array of I/O**
  - Wide range of external multi-standard I/O
  - High performance integrated serial transceivers
  - Analog-to-Digital converter inputs
Embedded Design Flow Using Zynq-7000

- **Industry-Leading Tools**
  - Xilinx SDK
  - ARM Ecosystem

- **Many Sources of SW IP**
  - Standardized around AMBA-AXI
  - Xilinx, ARM libraries
  - 3rd Parties

- **Industry-Leading Tools**
  - C-Gates / AutoESL
  - System Generator
  - VHDL/Verilog

- **Many Sources of HW IP**
  - Standardized around AXI
  - 3rd Parties
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Agile Mixed-Signal Integration

Flexible general purpose analog interface
- Integrated with all 7 series FPGAs and Zynq

Supports broad range of applications
- From simple monitoring to complex signal processing

Embedded temperature and supply sensors
- Enhance reliability, security and safety

- Dual 12-bit 1Mps Analog-to-Digital Converters
  - ADCs carry out 16-bit conversion with digital calibration
  - ADC specified over full industrial range -40°C to +100°C
  - DNL ±0.9 LSBs, INL ±2 LSBs, Gain Error ±0.4%, Offset ±4 LSBs

- Dual Independent Track & Hold (T/H) Amplifiers
  - Precise user control of sampling instant & simultaneous sampling
  - Signal acquisition during conversion increases multiplexed throughput rate
  - Track & Holds supports true differential sampling
  - Track & Holds can be configured to support unipolar & bipolar signals

- On-chip Voltage Reference
  - ±1% from -40°C to +100°C
  - External reference input option

- On-Chip Thermal and Supply Sensors
  - Temperature sensors with ±4°C error from -40°C to +100°C
  - Power supply monitoring with ±1% error from -40°C to +100°C
  - Automatic over temperature power down

- External Analog Input Channels
  - One dedicated input channel for use with external analog multiplexer
  - Up to 17 analog inputs supported using dual purpose digital IO
Build better systems with fewer chips... faster

Programmable Systems Integration

- Increased System Performance
- BOM Cost Reduction
- Total Power Reduction

Accelerated Design Productivity

ARTIX™ | KINTEX™ | VIRTEX™ | ZYNQ™ | VIVADO.™
Total Power Reduction

50% FPGA Power Savings

5 Key FPGA Power Innovations

- Optimized & Simpler HPL
- Re-architected Transceivers
- Multi-mode I/O Control
- Intelligent Clock Gating
- Voltage Scaling/Power Binning

50-70% System-Level Power Savings

Zynq Enabled Low Power

SSIT Enabled Low Power

Programmable Systems Integration

BOM Cost Reduction

Total Power Reduction

Increased System Performance

Accelerated Design Productivity

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Programmable Components

- Systems
- Logic
- Microprocessors
- I/O
- Analog/Mixed Signal

It is **ALL PROGRAMMABLE**
Enabling the Next Decade of ALL PROGRAMMABLE Devices

Accelerating Integration

IP & System-centric integration with fast verification

Vivado next generation design system

RTL to Bit-stream with iterative approach

Fast, hierarchical and deterministic closure automation w/ ECO

Accelerating Implementation

up to 4X

1X

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Maximizing Design Reuse

Architecture Enabled IP Portability

Leveraging Standards for IP Reuse

Dramatically Reduce Time to Access, Reuse & Integrate World Class IP
Vivado: More Turns per Day, Ease-of-Use and Reuse

Vivado RTL->Bits

Vivado Run Time

Next Gen Architecture for Run-time, Memory Utilization & QoR

- Unified, streamlined, built for reuse
  - U/I based on PlanAhead
  - Simplified use models tailored to different user profiles
  - Industry standard formats
  - Hierarchical flows
  - Easy IP packaging and reuse
More Turns per Day with High-Level Synthesis

2-5X Step Function in Design Productivity vs RTL

C-based High-Level Synthesis

Time spent achieving design Functional correctness

Time spent verifying Implementation tools did Not insert errors

Optical flow video example

<table>
<thead>
<tr>
<th>Input</th>
<th>C Simulation Time</th>
<th>RTL Simulation Time</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 frames of video data</td>
<td>10 seconds</td>
<td>~2 days*</td>
<td>~12,000X</td>
</tr>
</tbody>
</table>

*RTL Simulations performed using ModelSim
Recent Innovation and Investment Timeline

Projects Began
- 2004: PlanAhead, SIRF
- 2005: AMS, AccelChip
- 2006: 28nm HPL
- 2007: Rodin, Targeted Design
- 2008: EPP, AXI, Plug & Play IP
- 2009: FMC, PowerLite
- 2010: AutoESL
- 2011: Omiino, Modelware, Sarance

Projects Delivered
- MatLab/Simulink, LabView
- IP-based Design
- PlanAhead with ISE Flow
- ISE Improvements
- TDPs

Investments Enable Innovation and Deliver Value
Xilinx Technology Evolution

Programmable Logic Devices
Enables Programmable
‘Logic’

ALL Programmable Devices
Enables Programmable
Systems ‘Integration’
The Road Ahead

- Programmable logic is not only about programmable logic.
- We are still gaining tremendous benefit from scaling. And we have additional technologies we can use.

We are still looking up
What Xilinx Makes Possible:

ALL PROGRAMMABLE

ALL Programmable Electronic Systems

ALL Programmable Technologies

ALL Programmable Devices