

(GECO)²

A Graphical Tool for the Generation of Configuration Bitstreams for a Smart Sensor Interface Based on Coarse-Grained Dynamically Reconfigurable Hardware



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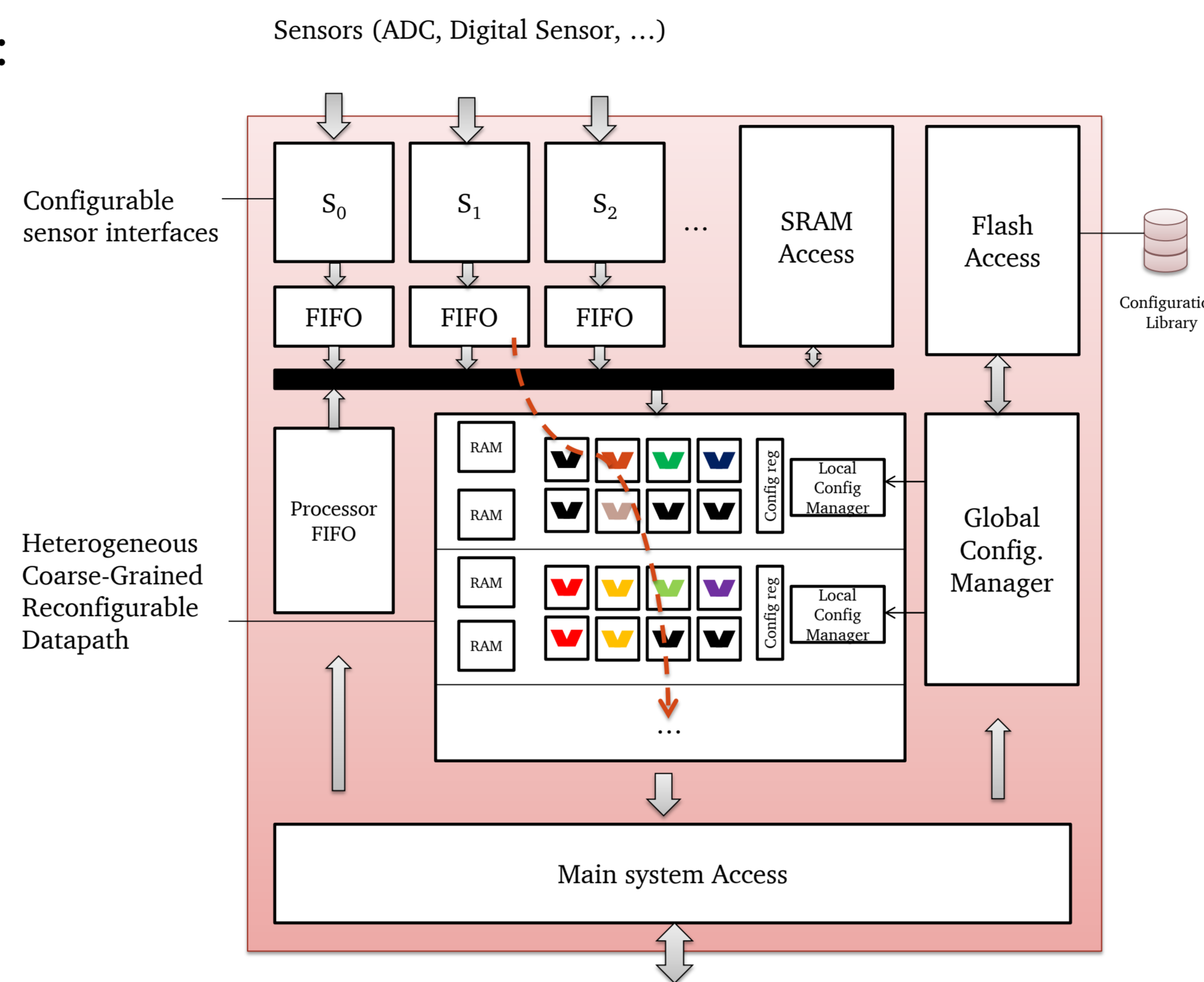
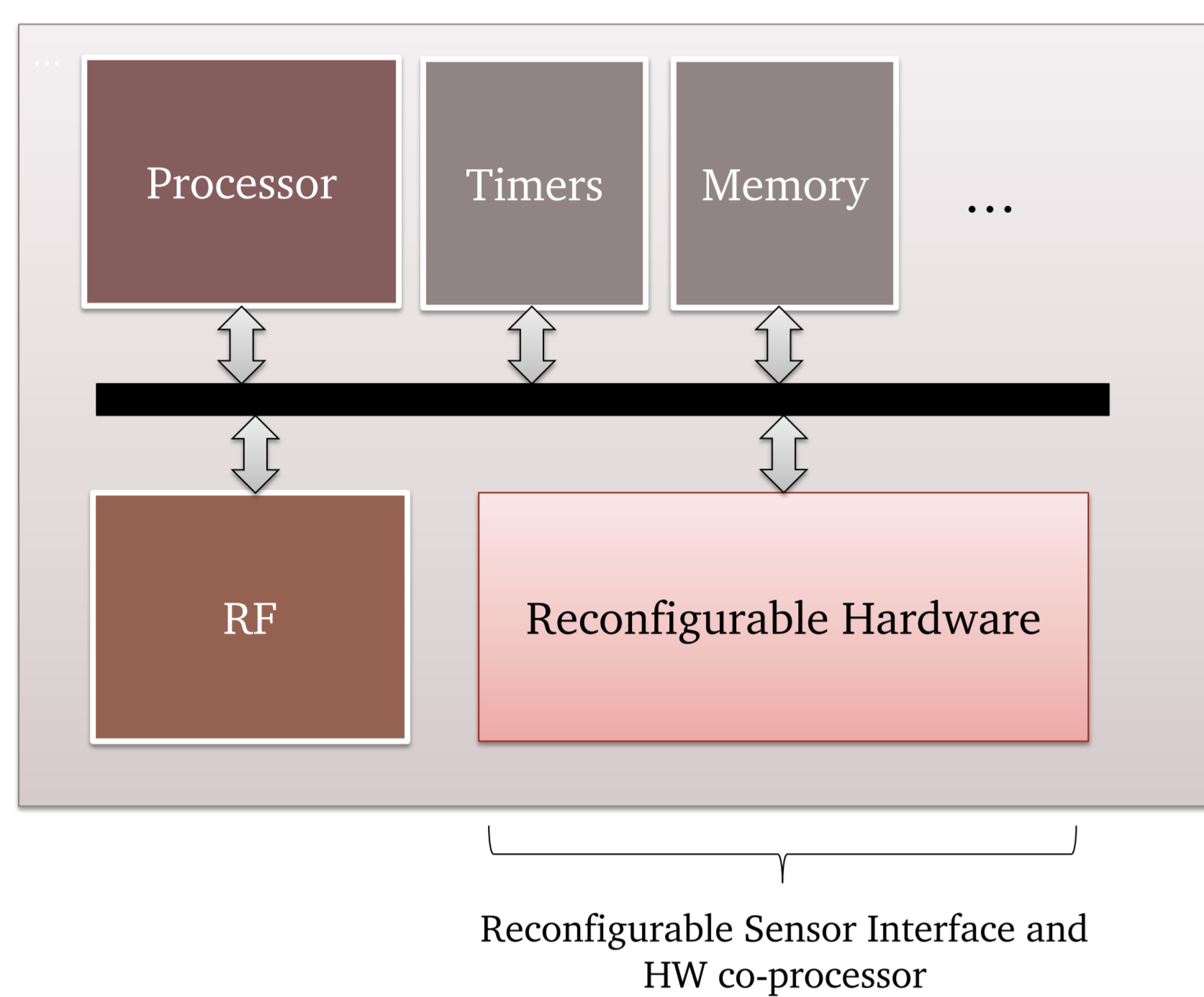
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Motivation

Rapid development of hardware accelerators for autonomous wireless smart sensor devices :



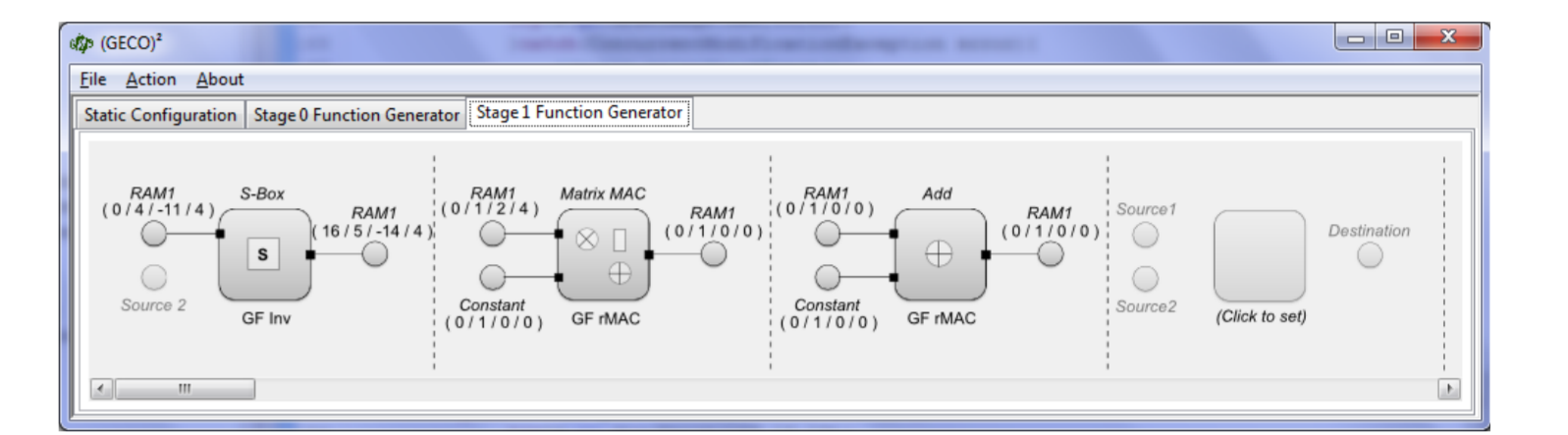
Suitable for energy efficient acceleration of computationally demanding tasks in WSNs :

- Sensor data preprocessing
- Feature Extraction
- Encryption / FEC
- ...

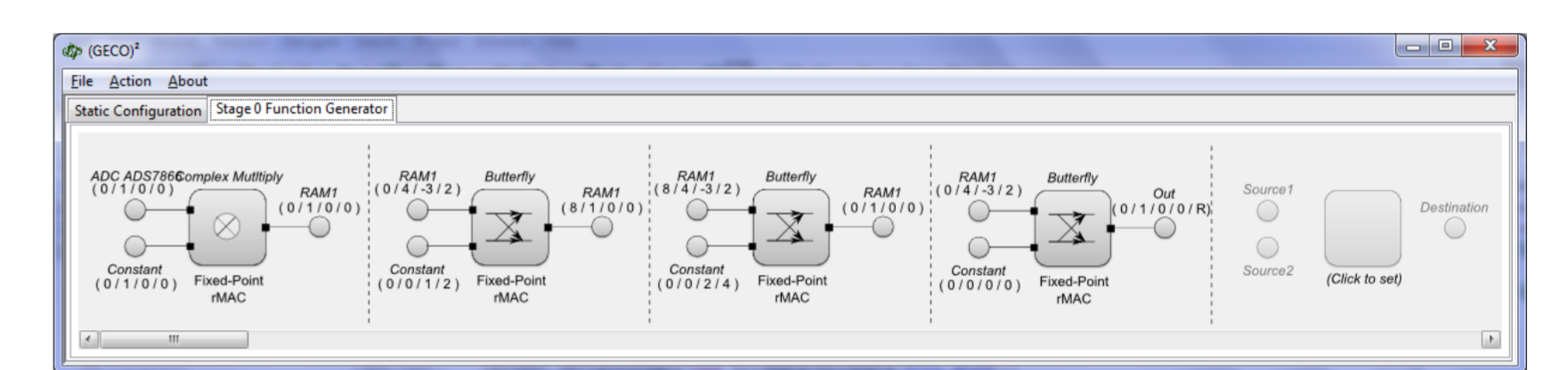
Requirements :

- **Flexibility** : each sensor network application has different sensors / processing algorithms
- **Performance**
- **Programmability**: WSN developers are not familiar with programmable logic design

(GECO)² Dynamic Configuration Editor

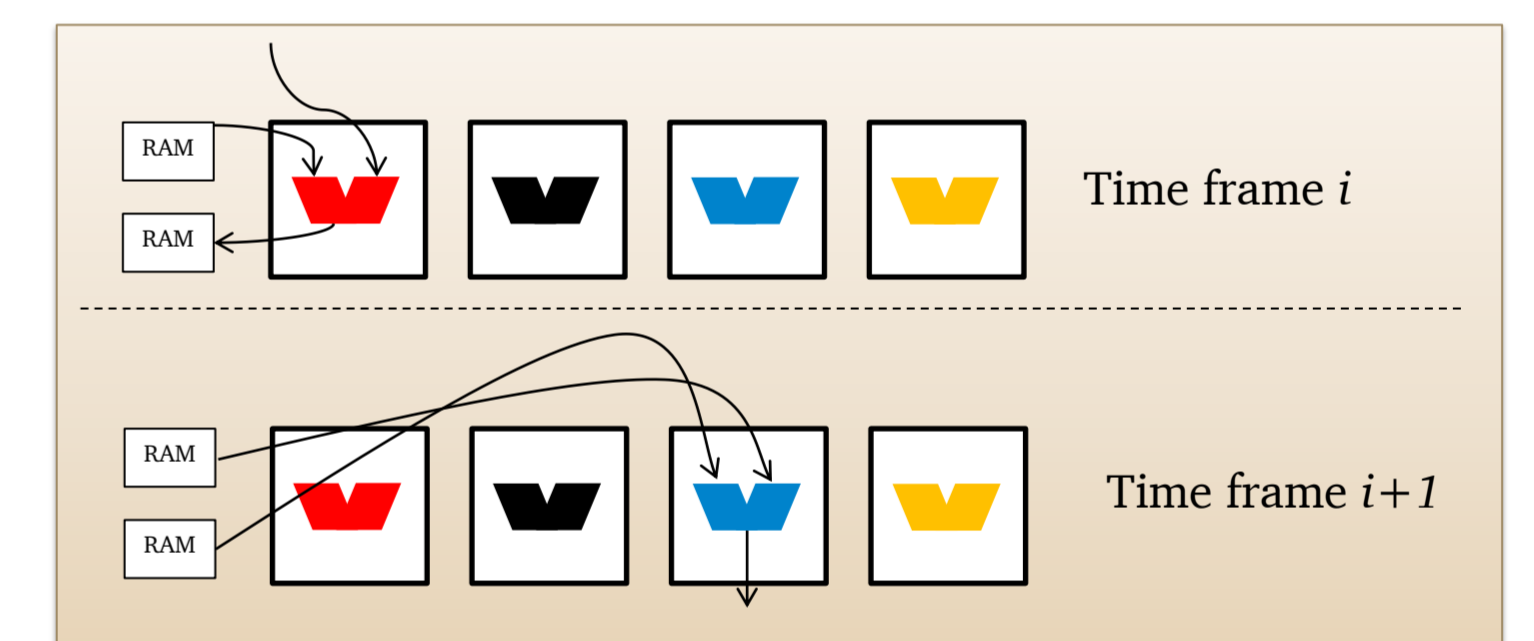


AES encryption round configuration



Fixed Point Radix 2 FFT configuration

- Graphical elaboration of data flows through reconfigurable operators
- Stream-based
- Sequential overview
- Editor for compilable microprogram to edit control flow of frames
- Automatically generate configuration bitstream compatible with static architecture defined in step (1)



- Sequences can be saved as function macro for further reuse
- Macro can be dynamically loaded on remote sensor node with compatible architecture



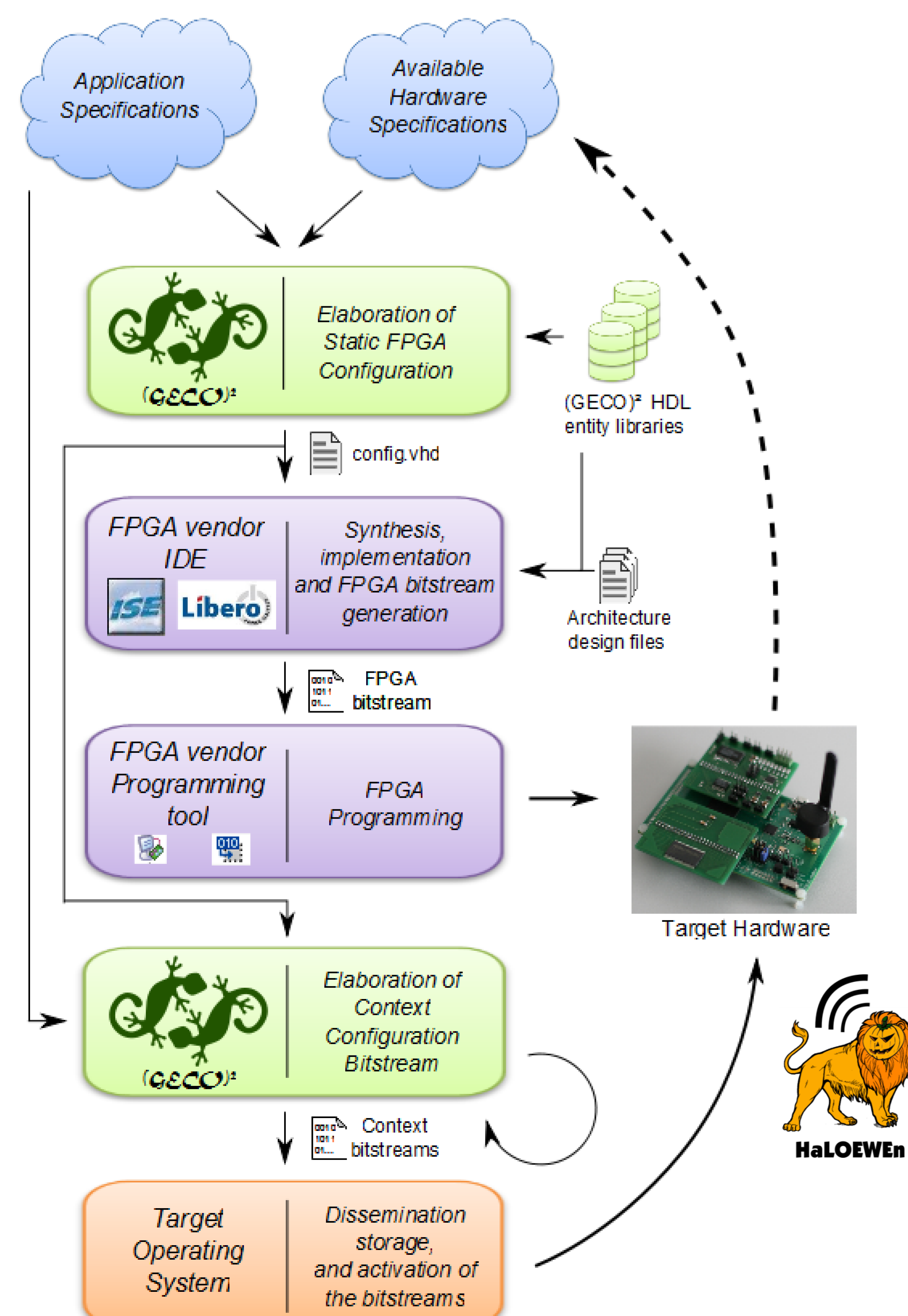
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2 steps

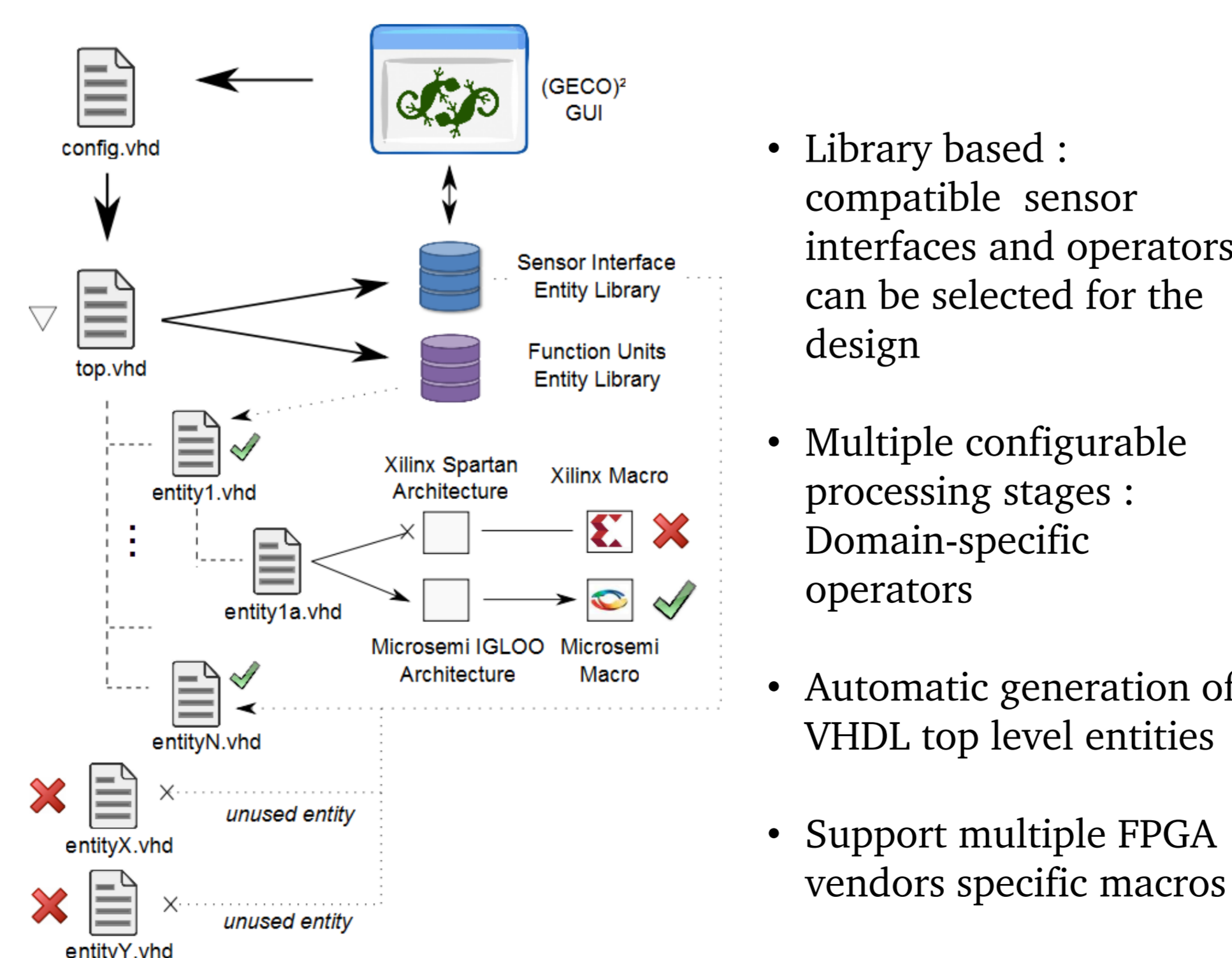
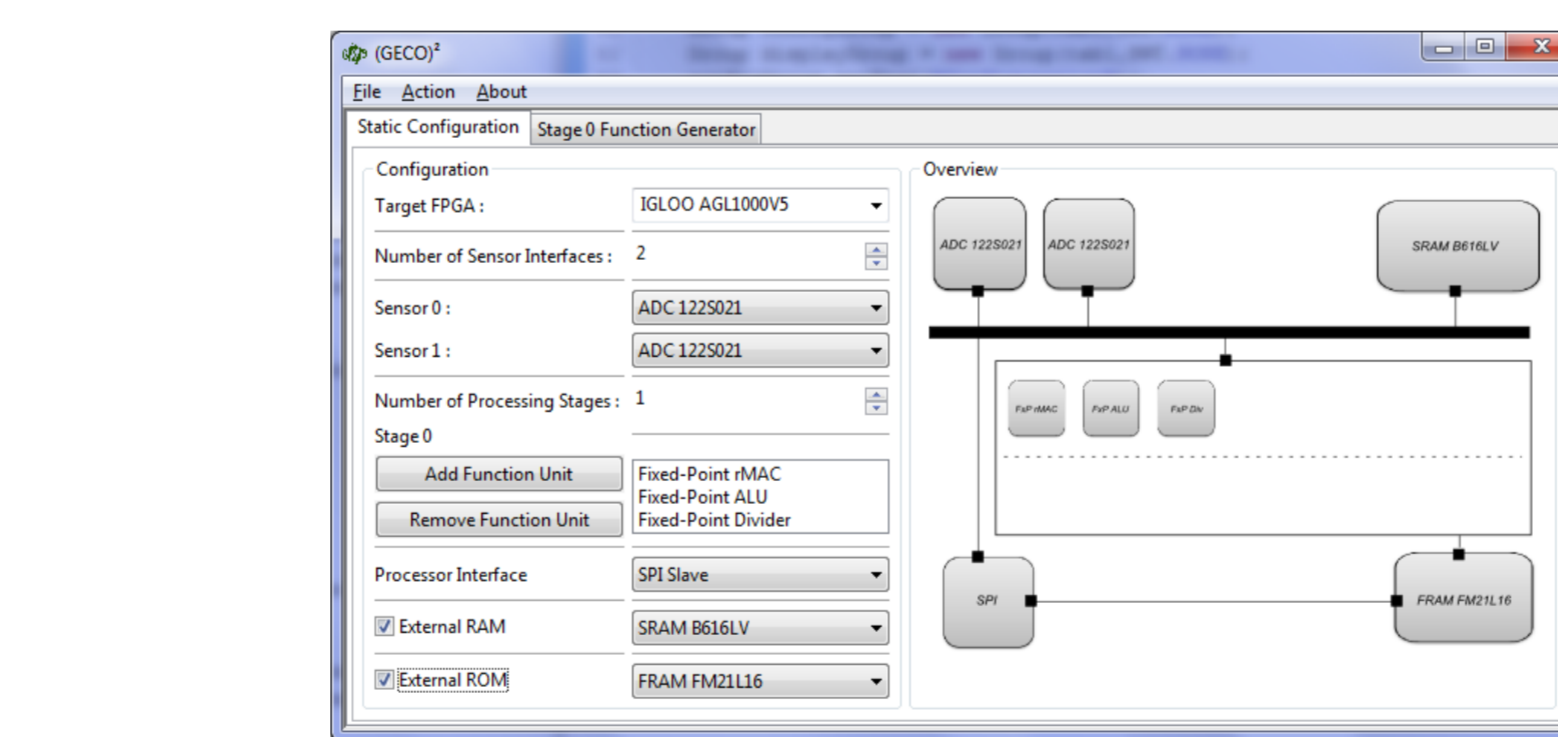
Graphical Environment for Configuration and Generation of bitstreams of Coarse-grained dynamically reconfigurable architectures

- 1. Static Configuration**
 - Application specific customization of datapath reconfigurable operators
 - Selection of HW sensor interfaces
- 2. Elaboration of dynamically loadable configurations corresponding to the static architecture**
 - Time-multiplexed streaming processes

(GECO)² Design Flow

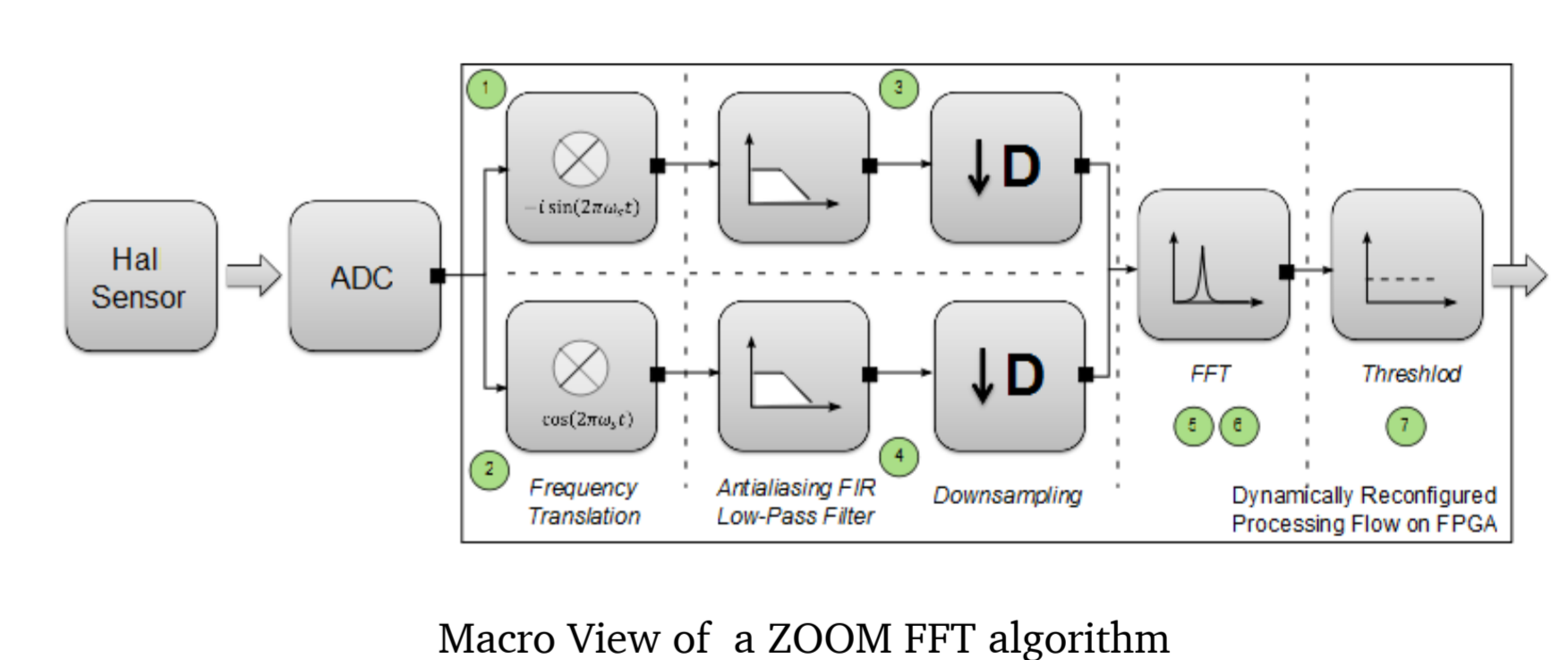


(GECO)² Static Design



- Library based : compatible sensor interfaces and operators can be selected for the design
- Multiple configurable processing stages : Domain-specific operators
- Automatic generation of VHDL top level entities
- Support multiple FPGA vendors specific macros

(GECO)² Usage



- Circled numbers indicate the sequence of macros dynamically configured in the datapath
- Rapid elaboration of high performance data processing HW accelerators enabled
- Suitable for low power high-bandwidth sensing devices

Acknowledgments

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